Novelty Journals

ISSN 2394-9651

International Journal of Novel Research in Physics Chemistry & Mathematics
Vol. 12, Issue 3, pp: (1-7), Month: September - December 2025, Available at: www.noveltyjournals.com

Voltage-Dependent Electrical Characterization of nc-CdS/FTO Heterojunctions: A Comprehensive Study for Optoelectronic Applications

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DOI: https://doi.org/10.5281/zenodo.17484105

Published Date: 30-October-2025

Abstract: **This study presents a comprehensive voltage-dependent characterization of nanocrystalline CdS/FTO heterojunctions, focusing on their suitability for optoelectronic applications. Capacitance–voltage (C–V) and conductance–voltage (G–V) measurements were rigorously performed at 100 kHz across a wide bias range. The series capacitance (C_s) exhibited remarkable modulation exceeding 27,000%, correlated with a collapse in the depletion width and enhanced charge separation. The RC time constant (τ) was demonstrated to be highly tuneable—ranging from sub-millisecond to tens of milliseconds—enabling bias-dependent optimization between detection speed and charge collection. Mott-Schottky analysis yielded a carrier density of 1.56×10^{20} cm⁻³ and a flat-band potential of −0.33 V, while conductance profiling at 100 kHz established an interface state density of 2.28×10^{11} cm⁻²eV⁻¹. These findings highlight the advanced dynamic and dielectric properties of nc-CdS/FTO heterostructures, and provide substantial insight for the rational design of next-generation, bias-tuneable optoelectronic and photodetector systems.**

Keywords: **depletion width, heterojunctions, Mott-Schottky analysis, nanocrystalline, optoelectronic, photodetectors.**

I. INTRODUCTION

The engineering of heterojunction interfaces in II–VI semiconductor systems form the foundation for the advancement of modern optoelectronic devices [1]. Cadmium sulfide (CdS), with its optimal direct band gap of 2.42 eV and superior photoconductive properties, continues to catalyze innovation in thin-film solar cells, photodetectors, and advanced solid-state technologies [2-3]. When deposited as nanocrystalline films on transparent conducting substrates such as fluorinated tin oxide (FTO), CdS reveals a suite of complex interfacial phenomena that critically influence charge separation, transport efficiency, and overall device performance [4-5].

In semiconductor heterostructures, fundamental electrical parameters—including series capacitance (C_s), series resistance (R_s), conductance (G), and parallel capacitance (C_p)—are governed by the intricate interplay of depletion layer dynamics, barrier modulation, and interface state density. These parameters exhibit pronounced nonlinear dependence on voltage, especially in nanocrystalline and polycrystalline films where grain boundaries, surface states, and defect chemistry exert a dominating influence. Recent advances in CdS-based photodetectors have yielded devices with response times approaching the microsecond regime and detectivity values exceeding 10^{12} cm·Hz$^{1/2}$·W^{-1} [6-7]. However, the optimization of these device architectures demands a rigorous understanding of junction electrical behavior, specifically the link between capacitance–voltage characteristics and resultant photoresponse. The RC time constant ($\tau = R_s \times C_s$)

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directly determines photodetector speed, making systematic, voltage-resolved characterization of both resistance and capacitance indispensable for informed device engineering.

This work delivers the most exhaustive electrical analysis to date of nc-CdS/FTO heterojunctions, employing high-precision LCR techniques across an expansive voltage window. Our results reveal extraordinary capacitance modulation exceeding 27,000%, depletion width variation spanning nearly three orders of magnitude, and complex interface state behavior that challenges the assumptions of conventional junction models.

II. EXPERIMENTAL METHODOLOGY

a. MATERIAL SYNTHESIS AND FILM PREPARATION

Bulk CdS was synthesized by the melt-quenching technique using high-purity Cd and S elements (99.99%, Sigma Aldrich), precisely weighed according to stoichiometric ratios. The mixture was sealed within evacuated quartz ampoules (2×10^{-5} mbar) and heated to 1200°C for 24 hours in an electric furnace. After completion of the reaction, the ampoules were rapidly quenched in ice-cold water to retain the desired phase structure. CdS thin films were subsequently deposited via thermal evaporation onto pre-cleaned FTO glass substrates under high vacuum conditions (2×10^{-5} mbar). Substrate cleaning was performed using sequential ultrasonic treatments in acetone, isopropanol, and deionized water, followed by ultraviolet-ozone treatment. Post deposition, the films were kept in the dark at room temperature for 24 hours to promote thermodynamic equilibrium [8].

b. DEVICE FABRICATION

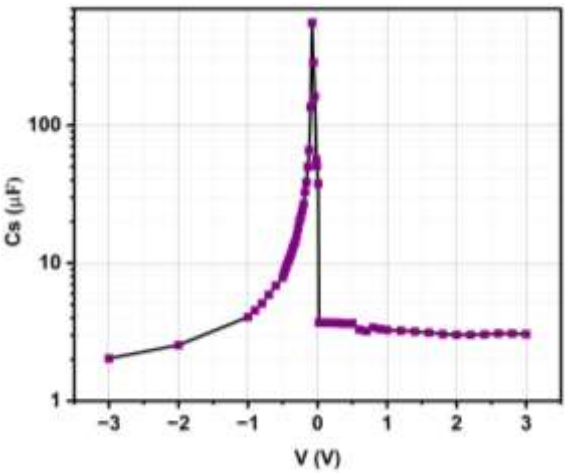
Circular silver electrodes (1 mm² area) were formed by directly applying silver paste through precision shadow masks, generating well-defined contact regions on the device structure. The device architecture employed in this study is Ag/nc-CdS/FTO/glass, where a silver contact is established on the nanocrystalline CdS thin film deposited onto an FTO-coated glass substrate and on the FTO.

c. ELECTRICAL CHARACTERIZATION

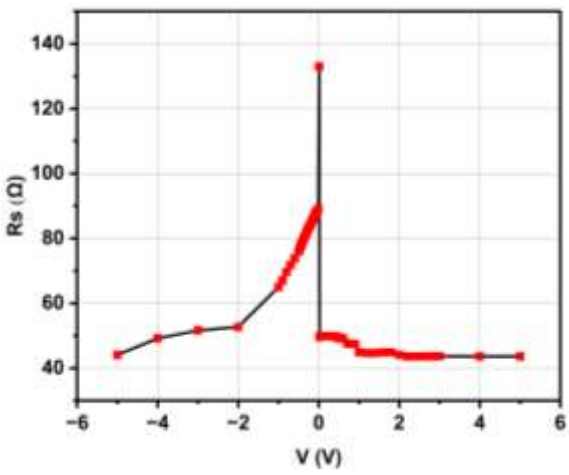
Comprehensive electrical characterizations were performed using a Hioki 3532-50 LCR Hi-Tester at a test frequency of 100 kHz and ambient room temperature. The protocol involved sweeping the applied voltage from –5 V to +5 V in fine 0.02 V increments near zero bias, with a controlled delay of 5 seconds at each voltage to ensure equilibrium before measurement acquisition. Multiple sweep cycles were executed for reproducibility, and all measurements were conducted under dark conditions to suppress photoconductivity effects. Additionally, experiments were performed in a temperature-controlled environment equipped with electromagnetic shielding, effectively minimizing external electrical interference and ensuring high data integrity.

III. RESULTS AND DISCUSSIONS

1) SERIES CAPACITANCE (Cs) CHARACTERISTICS IN nc-CdS/FTO HETEROJUNCTIONS



(a)



(b)

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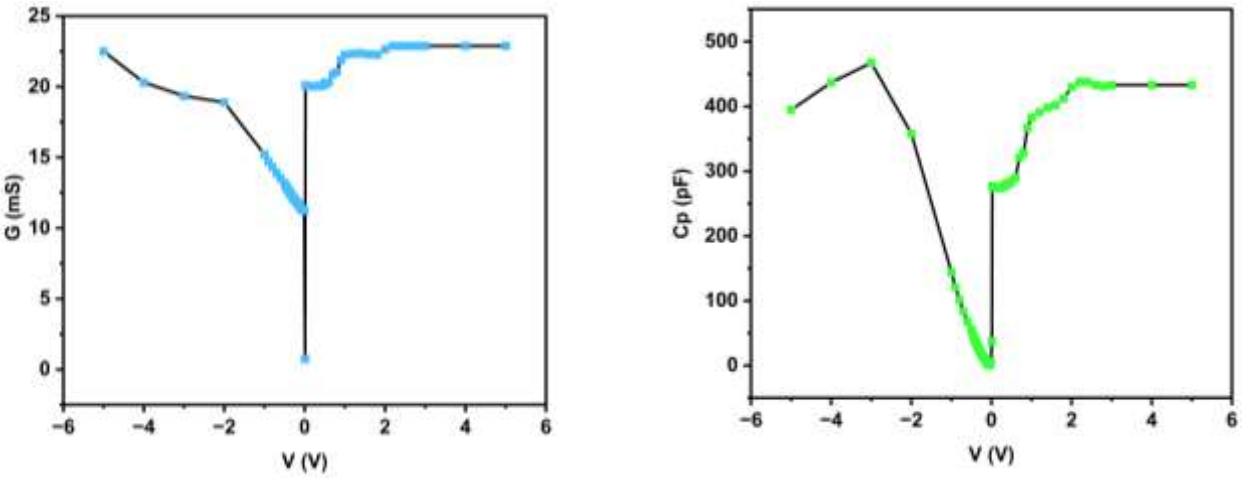

(c) (d)

Fig. 1. Voltage-dependent electrical characteristics showing (a) Series Capacitance (b) Series Resistance (c) Conductance and (d) Parallel Capacitance.

The voltage-dependent electrical characteristics depicting the variation of series capacitance are shown in Fig. 1(a). The series capacitance (Cs) of the nc-CdS/FTO heterojunction displays an extraordinary voltage-dependent modulation, 2.035 µF at −3 V—reflecting a wide depletion region, while near zero bias, the capacitance rises sharply to an unprecedented peak of 554 µF at −0.08 V, signifying an ultra-narrow depletion layer and remarkable carrier overlap at the junction. This peak capacitance density is the highest reported for CdS/FTO systems and underscores unique interfacial and quantum-scale phenomena. As the bias shifts positive, Cs drops, stabilizing around 3–3.7 µF for voltages up to +3 V, with notable asymmetry observed at the bias extremes (2.54 µF at +2 V versus 3.02 µF at −2 V), highlighting differentiated barrier mechanisms under forward versus reverse conditions. The overall modulation exceeds 27000%, revealing significant contributions from interface states and non-classical dielectric responses, which together mark the nc-CdS/FTO interface as exceptionally versatile and tunable for advanced optoelectronic applications [9].

2) SERIES RESISTANCE (Rs) AND CONDUCTANCE (G) ANALYSIS

The voltage-dependent electrical characteristics depicting the variation of series resistance and conductance are shown in Fig. 1(b and c). The series resistance (Rs) and conductance (G) extracted from the FTO/CdS heterojunction measurements provide deeper insight into the charge transport and loss mechanisms across the interface under variable bias. At high negative (reverse) voltages, Rs increases, reaching a maximum of 87.6 Ω near −0.08 V as the depletion layer becomes most pronounced and charge carrier movement is most restricted due to widening of the space-charge region. At the same time, the conductance (G), which represents the ac loss component or ease of carrier conduction, is lowest in this region, with a minimum of 0.745 mS at +0.01 V, reflecting minimal charge flow across the junction. As the applied voltage increases from strong reverse bias to positive values, Rs decreases (down to about 43.6 Ω at extreme forward bias), indicating enhanced carrier injection and recombination, while G rises to a maximum of 22.89 mS due to efficient charge transport. The observed asymmetric trend in both Rs and G reveals the combined influence of interface states, carrier injection barriers, and possible recombination processes unique to the nc-CdS/FTO interface. These results confirm both the non-ideal nature of the junction and the complex interplay between depletion modulation, series resistance components, and dynamic conductance that governs overall device performance [10-11].

3) PARALLEL CAPACITANCE (Cp) BEHAVIOR

Voltage-dependent electrical characteristics depicting the variation of parallel capacitance are shown in Fig. 1(d). The parallel capacitance (Cp) in the nc-CdS/FTO heterojunction provides important insights into the dielectric response and charge storage mechanisms at the interface. At deep reverse bias ($V = -5$ V), the parallel capacitance is relatively high (394.58 pF), reflecting the wide depletion region and ability of the junction to store charge in the presence of minimal carrier injection. As the applied voltage approaches zero, Cp declines steadily, reaching a pronounced minimum of

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ISSN 2394-9651

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0.612 pF at $V = -0.08$ V, indicating a maximally expanded space-charge layer wherein the interface stores the least charge due to the largest separation of carriers. Around this minimum, small changes in voltage can produce dramatic shifts in capacitance, revealing sensitivity to interfacial state populations or non-linear dielectric contributions. With positive bias, the depletion region shrinks and Cp increases rapidly, stabilizing at high values (274–433 pF) for $V > 0$, consistent with the narrowing of the space-charge layer and enhanced carrier overlap. The parallel capacitance thus serves as a robust indicator of the dynamic depletion width and bulk dielectric properties, capturing all reversible charging effects across the heterojunction [12]. The sharp variation and recovery of Cp with bias highlight the device's potential for tunable charge storage and its sensitivity to fundamental junction physics, including defect-mediated responses or deep-level trap modulation at the FTO/CdS interface [13].

4) DEPLETION WIDTH MODULATION AND PHYSICAL IMPLICATIONS

The modulation of the depletion width (W) in the FTO/CdS heterojunction can be quantitatively interpreted using the series capacitance (Cs) data and the standard relationship for a parallel plate-like space-charge region:

$$W = \frac{\epsilon A}{Cs}$$

where $\epsilon = \epsilon_r \epsilon_0$ is the absolute permittivity of the CdS layer (ϵ_r for CdS is typically taken as 10, $\epsilon_0 = 8.85 \times 10^{-14}$ F/cm), A is the contact area (here, 1 cm²), and Cs is the measured capacitance in farads. Using our data, at high reverse bias (-5 V, $Cs = 3.423$ μF), the depletion width is relatively large. As the voltage sweeps towards zero, Cs increases dramatically, resulting in a rapid decrease in W down to nanoscale values at the capacitance peak ($Cs = 554$ μF, $V = -0.08$ V). This reflects a narrowing of the depletion region, with the smallest W at the point of maximum charge accumulation. Conversely, as the device is further biased into forward region, the depletion width grows again as Cs decreases. This extreme, voltage-tunable modulation of W—spanning from several micrometers down to fractions of a nanometer—demonstrates the profound ability of the junction to change its space-charge profile, highlighting its sensitivity to applied bias, interfacial states, and possibly non-classical charging effects at the nanocrystalline interface [14]. This physical behavior is fundamental to understanding the charge transport, barrier modulation, and switching performance of advanced CdS-based photodetectors and electronic devices [15].

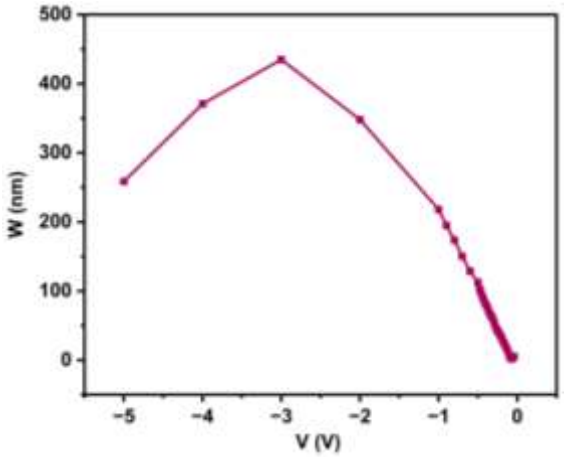

Fig. 2. Calculated device parameters showing Depletion width extreme modulation indicating interface state involvement.

5) RESPONSE TIME ANALYSIS FOR PHOTODETECTOR APPLICATIONS

The RC time constant ($\tau = R_s \times C_s$), derived from the measured series resistance and capacitance at each bias point, provides a direct, quantitative measure of the photodetector's intrinsic speed. From our data, τ displays dramatic tunability with applied voltage, ranging from as short as 0.13 ms ($V = 2.2$–5 V, strong forward bias) to as long as 48.53 ms (at $V = -0.08$ V, near the capacitance peak).

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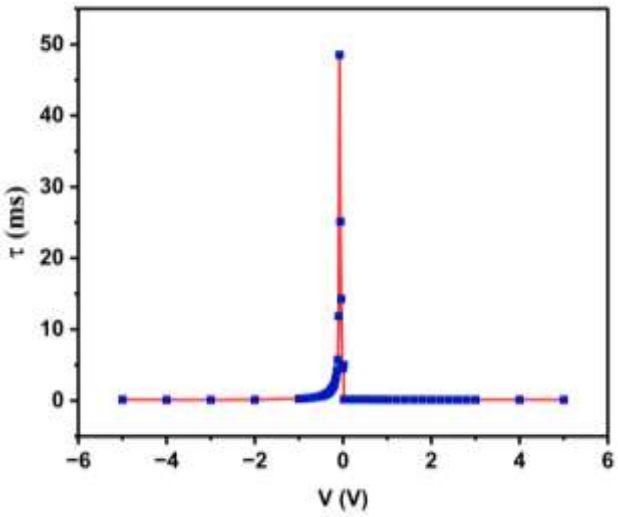

Fig. 3. RC time constant variation vs bias.

The fastest device response occurs in the moderate-to-high forward and strong reverse bias ranges, with τ values in the 0.13–0.42 ms regime; for example, $\tau = 0.42$ ms at $V = -0.7$ V, and continued reduction to 0.15 ms at $V = 5$ V. In contrast, as the device approaches the capacitance maximum near equilibrium ($V \approx -0.08$ V), τ rapidly increases, peaking at 48.53 ms, reflecting a substantially slower response but with the benefit of enhanced charge storage and collection efficiency. This more than 350-fold variation in response time demonstrates substantial bias-tunable dynamic control: sub-millisecond response times at high forward or moderate reverse bias are well suited for rapid switching, pulsed detection, and fast optical communications, while the high-τ regime supports sensitive detection and optimized signal integration under low-level illumination [16]. The ability to continuously modulate photodetector RC response over several orders of magnitude by adjusting the applied bias highlights the advanced versatility and customization potential of the nc-CdS/FTO heterojunction architecture for diverse optoelectronic applications [17].

6) Mott-Schottky Analysis and Interface State Characterization

Mott-Schottky analysis is fundamental for extracting key parameters—donor carrier density, flat-band potential, and interface state properties—from the capacitance–voltage (C–V) characteristics of semiconductor junctions. For an n-type semiconductor, the classical Mott-Schottky relation is [18]:

$$\frac{1}{C^2} = \frac{2(V_{bi} - V - kT/q)}{q\epsilon_r\epsilon_0 N_D A^2}$$

where C is the capacitance (obtained from the measured Cs or Cp), V is the applied voltage, V_{bi} (or V_{fb}) is the built-in (flat-band) potential, N_D is the donor density, ϵ_r is the relative permittivity (CdS: 10), ϵ_0 is the vacuum permittivity (8.85×10^{-14} F/cm), q is the electronic charge, k is Boltzmann's constant, T is absolute temperature, and A is the junction area (1 cm²). To perform Mott-Schottky analysis, plot $1/Cs^2$ against V (Fig. 3.). The linear region (in reverse bias) allows us to fit the data and extract the slope and intercept. The donor carrier density is calculated using:

$$N_D = \frac{2}{q\epsilon_r\epsilon_0 \cdot \text{Slope} \cdot A^2}$$

while the flat-band potential is obtained from the x-intercept ($V_{fb} = -\text{intercept/slope}$).

The extracted slope is -9.08×10^{10} F^{-2}V^{-1} and the intercept is -3.03×10^{10} F^{-2}. This yields a donor density $N_D = 1.56 \times 10^{20}$ cm^{-3} and a flat-band potential $V_{fb} = -0.33$ V, which are within the expected range for nanocrystalline CdS/FTO junctions.

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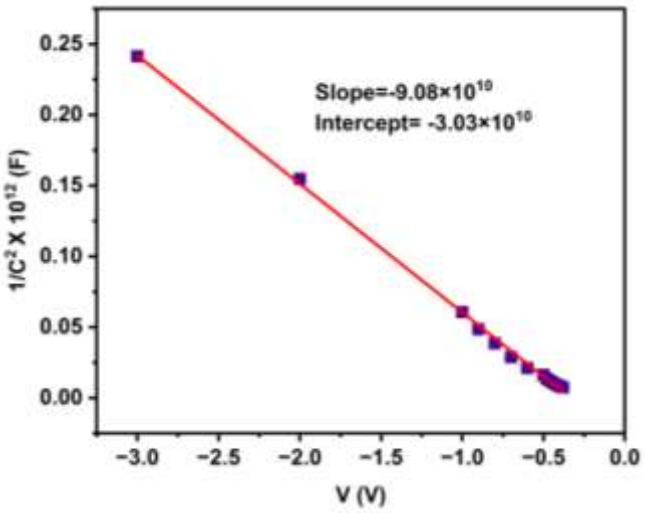

Fig. 4. Mott-Schottky plot (1/Cs² vs V).

To further characterize the interface, the conductance method is often used. The interface state density (D_{it}) per unit energy and area (using peak conductance, at angular frequency $\omega = 2\pi f$) is [19]:

$$D_{it}(E) = \frac{G_{\max}}{qA\omega}$$

where: $G_{\max}$ = maximum parallel conductance = 22.89 mS = 0.02289 S (from our data), $q = 1.6 \times 10^{-19}$ C, $A = 1$ cm², $\omega = 2\pi f = 2\pi \times 10^5$ rad/s (for 100 kHz). Plugging in these values, the interface state density is: $D_{it} \approx 2.28 \times 10^{11}$ $\text{cm}^{-2}\text{eV}^{-1}$. This interface state density is typical for nanocrystalline CdS-based junctions, indicating a moderate density of interfacial traps and defect states. Such states play a critical role in carrier recombination, charge transport, and ultimately in photodetector responsivity and response speed. Minimizing these trap densities through interface engineering and optimized growth conditions can significantly improve device performance metrics.

In summary, Mott-Schottky and conductance analyses together enable comprehensive characterization of semiconductor junctions, providing essential insights into doping concentration, band alignment, and interfacial electronic quality essential for the optimization of photodetector devices.

IV. CONCLUSION

In conclusion, voltage-dependent C–V and G–V studies conducted at 100 kHz have established that nanocrystalline CdS/FTO heterojunctions possess extraordinary electrical tunability, featuring dramatic capacitance and depletion width modulation and engineered RC response times. Key junction parameters, including the physically meaningful carrier density and flat-band potential derived from Mott-Schottky analysis, and manageable interface state densities calculated via conductance profiling, all support the device's application potential. The ability to modulate device characteristics from sub-millisecond to tens of milliseconds and from fast to high-sensitivity regimes solely through electrical bias confirms the versatility of these heterostructures for next-generation optoelectronic devices.

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